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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/347,690	07/02/1999	MANPREET S. KHAIRA	884.107US1	4194

7590 08/27/2002

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EXAMINER
MAKHDOOM, SAMARINA

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 08/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/347,690	KHAIRA ET AL.
	Examiner	Art Unit
	Samarina Makhdoom	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *02 July 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Figures 1, 3, and 9 should be labeled as "Prior Art." See the Casas et al. reference in the applicant's information disclosure statement.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 12-13 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

These claims contain the language 'less than about' and are not clear as to the limitations of the claims.

Inventorship

4. The present application names six joint inventors. The art submitted in the Information Disclosure Statement titled: Logic Verification of Very Large Circuits using Shark, names seven authors, six of them named on the present invention and describes the same material as disclosed

in the present application. T. Tetzlaff is missing from the application. Examiner would like to know if T. Tetzlaff contributed to the claimed invention.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-28 are rejected under 35 U.S.C. 102(a) as being anticipated by Casas, et al., "Logic Verification of Very Large Circuits Using Shark", Twelfth International Proceeding on VLSI Design, Jan 7-10, 1999.

As per Claim 1, Casas et al. disclosed a method of decomposing a circuit into a plurality of extended latch boundary components and partitioning the components, (See Page 311, Top of Left Column).

As per Claim 2, Casas et al. disclose decomposing the extended latch boundary components, (See Page 312, Bottom of Left Column).

As per Claims 3-10, Casas et al. disclose using a constructive bin-packing heuristic, merging the extended latch boundary components, and partitioning by hierarchical cells, and achieving load balancing (See Page 311, Top of Right Column).

As per Claims 11-16, Casas et al. disclose partitioning the circuit to achieve maximum speed up, minimize logic replication and cut size. (See Page 311, Section 3.1).

As per Claim 17, Casas et al. disclose the latch boundary component path selected from a group of latches and primary outputs, (See Page 312, Section 3.2)

As per Claims 18-20, Casas et al. disclose the method of grafting the expanded circuit structure (See page 312, Section 3.5)

As per Claims 21-23, Casas et al. disclose preparing, adjusting and executing simulations. (See Page 313, Section 3.4)

As per Claims 24-28, Casas et al. disclose a computer system with a processor unit, dicing unit and simulation unit. (See Page 310, Figure 1 and related text).

7. Claims 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Casas, et al., "Logic Verification of Very Large Circuits Using Shark", Twelfth International Proceeding on VLSI Design, Jan 7-10, 1999.

As per Claim 1, Casas et al. disclosed a method of decomposing a circuit into a plurality of extended latch boundary components and partitioning the components, (See Page 311, Top of Left Column).

As per Claim 2, Casas et al. disclose decomposing the extended latch boundary components, (See Page 312, Bottom of Left Column).

As per Claims 3-10, Casas et al. disclose using a constructive bin-packing heuristic, merging the extended latch boundary components, and partitioning by hierarchical cells, and achieving load balancing (See Page 311, Top of Right Column).

As per Claims 11-16, Casas et al. disclose partitioning the circuit to achieve maximum speed up, minimize logic replication and cut size. (See Page 311, Section 3.1).

As per Claim 17, Casas et al. disclose the latch boundary component path selected from a group of latches and primary outputs, (See Page 312, Section 3.2)

As per Claims 18-20, Casas et al. disclose the method of grafting the expanded circuit structure (See page 312, Section 3.5)

As per Claims 21-23, Casas et al. disclose preparing, adjusting and executing simulations. (See Page 313, Section 3.4)

As per Claims 24-28, Casas et al. disclose a computer system with a processor unit, dicing unit and simulation unit. (See Page 310, Figure 1 and related text).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hashizume et al, U.S. Patent No. 5,260,949, discloses scan path system and an integrated circuit device.

K. Hering, R. Haupt, Th. Villman, "Hierarchical Strategy of Model Partitioning for VLSI-Design Using an Improved Mixture of Experts Approach." Parallel and Distributed Simulation, 1996. Pads 96. Proceedings. Tenth Workshop on, 1996 Page(s): 106 –113

M. L. Bailey, J. V. Briner, Jr., R. D. Chamberlain, "Parallel Logic Simulation of VLSI Systems," ACM Computing Surveys, Vol. 26, No. 3, September 1994.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samarina Makhdoom whose telephone number is 703-305-7209. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J. Teska can be reached on 703-305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0040 for regular communications and 703-305-0040 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

SM
August 23, 2002

Wm Thomson
A.U 2123